Connecting wire-based solar cells without any transparent conducting electrode
Connecting wire-based solar cells without any transparent conducting electrode†

Le Duc Toan, Eric Moyen, Mihai Robert Zamfir, Young Woo Kim, Jemee Joe, Young Hee Lee and Didier Pribat

In order to reduce substrate costs and increase light absorption, solar cells based on semiconductor wire arrays are currently being actively studied. Whether built with Si, InP or other semiconductor materials, wire-based cells invariably use a transparent conductive coating for one of the electrodes, which complicates the processing and does not contribute to the reduction of the overall cost of the cell. Here, we propose a totally novel connection process, where the transparent conductive electrode is replaced with an array of in situ grown metallic nanowires. During their growth, these metallic nanowires randomly connect to core–shell p-i-n Si wires previously synthesized by chemical vapor deposition. We demonstrate the feasibility of this new random connection concept by using a coplanar solar cell design with interdigitated base and emitter contacts. We obtain a high fill factor of ~74% and efficiencies of 4.5% with only 33% of the surface covered by p-i-n Si wires.

Because of improved light absorption and trapping, as well as use of less semiconductor materials, solar cells based on arrays of semiconductor wires have the potential to improve efficiency while decreasing costs. Over the past few years, such cells have seen their efficiency increase steadily, now reaching 13.8% for InP nanowire arrays. Among wire-based solar cells, those which make use of Si micro/nanowire arrays are the most studied. Schematically, there are two types of solar cells based on Si wire arrays, depending on whether hydrogenated amorphous silicon (a-Si:H) is used in the structure or not. Cells based only on crystalline silicon (c-Si) potentially combine the advantages of c-Si, such as stability, long lifetime, low toxicity, abundance, etc. with those of cheaper thin film technologies (less material use, lower processing temperatures, etc.). Efficiencies of ~8% have been reported for such cells based on c-Si core–shell p-n wire arrays grown by the vapor–liquid–solid (VLS) process in a chemical vapor deposition (CVD) reactor. Moreover, it has been predicted that those cells could reach efficiencies higher than 17% using only a small percentage of the Si volume of the wafer-type cells. Another approach for solar cells based on Si wire arrays makes use of VLS c-Si cores on which a-Si:H shells are deposited; these cells incorporate a heterojunction between c-Si and a-Si:H and they usually deliver a higher open circuit voltage (VOC) than their all-c-Si counterparts. Multi-walled carbon nanotube cores have also been used instead of the c-Si ones. Wire-based solar cells with a-Si:H shells are usually grown at (much) lower temperature than the all-c-Si ones and they reach 8–9% efficiency values. At this point, we note that wire-based solar cells made by etching monocrystalline wafers exhibit higher efficiencies around 10%. However, the economic interest of such cells is rather poor compared to those made with CVD-grown wires, because of the high cost of monocrystalline Si wafers.

A common feature of these wire-based cells, whether built with Si or other semiconductor materials, is the use of a transparent conducting oxide (TCO) film for one of the contacts. The most popular TCO is indium-tin oxide (ITO), which is an expensive material due to the scarcity of In. It is recognized that suppressing the transparent coating (ITO or some other transparent oxide mixture, see ref. 11) would be a great step towards cost reduction of thin film-type solar cells. The TCO film can be deposited either on the planarized wire array or by conformal coating over the wires. Planarization comes with a cost, since it requires extra processing steps. Moreover, introducing a planar TCO interface increases reflection losses by a few percent. On the other hand, because of shadowing effects during deposition, conformal coating of high aspect ratio wires is not an easy task, particularly on dense NW arrays and on large areas. To summarize, there are some real drawbacks in using

† Electronic supplementary information (ESI) available: Growth, electrical and structural characterization of the p-n and NSi, wires, details about the band diagram, the evaluation of series resistances and the effective area of the device. See DOI: 10.1039/c5ce01786f

Department of Energy Science (DOES), Sungkyunkwan University, Suwon, 440-746, Republic of Korea. E-mail: prbat2@yahoo.fr

Center for Integrated Nanoscience and Physics (CINAP), Institute for Basic Science (IBS), Suwon 440-746, Republic of Korea

This journal is © The Royal Society of Chemistry 2016

CrystEngComm, 2016, 18, 207–212 | 207
TCOs, but so far there are few other options if one wants to obtain a low series resistance for the cell.

In this report, we propose a totally new method of connecting the semiconducting wires, which suppresses the need for ITO or any other transparent conducting coating and does not require any planarization. The idea is to use an array of metallic nanowires (NWs) to randomly connect the semiconductor-based (e.g., Si) active wires. Maybe the connection principle will be better understood with the help of Fig. 1. The coplanar solar cell architecture is composed of, first, a family of core–shell silicon wires with a p-n or p-i-n structure. The core c-Si wires are first grown by CVD using a VLS process and they are anchored and connected at their roots to a network of finger-like electrodes (the base contact); the shell layers are deposited during the same pump-down by changing the temperature as well as the gas mixtures (e.g., for a different doping) and flow rates. After deposition of the shell layers, the substrates are removed from the CVD reactor and a nickel (Ni) film is deposited and patterned between the fingers supporting the Si wires, thus forming a second array of coplanar electrodes interdigitated with the first one (the emitter contact). A random array of nickel silicide (NiSi) NWs is then grown from the Ni stripes during a second CVD step. Under certain process conditions, these NiSi, NWs grow spontaneously when a Ni film is exposed to a silicon-bearing gas (e.g., SiH₄) at ~400 °C in a CVD reactor. During the course of their growth, the NiSi, NWs randomly come into contact with the previously grown p-n or p-i-n core–shell Si wires, thus establishing the second electrical connection of the solar cell. Fig. 1 shows various views of a device using the novel connection process that we propose here. Fig. 1a presents a schematic perspective drawing of the interdigitated coplanar structure after growth. A scanning electron microscopy image of a completed device is shown in Fig. 1b (top view). For this device, the width of the fingers (whether Al or Ni) is 10 μm and their length is 100 μm; the spacing between the fingers of opposite electrodes is 5 μm. Note that we have explored a few other device geometries, particularly with larger spacing between opposite electrodes (see below).

Fig. 1 (panels c and d) shows the enlarged views of the connecting regions between the p-i-n Si wires and the NiSi, NWs.

In order to simplify the overall solar cell fabrication process, we have used an aluminium (Al) thin film (~300 nm thick) for the growth of the core Si wires (Fig. S1, ESI†). This Al film is not totally consumed during the growth step, thus it also serves as a base electrode for the solar cell. Moreover, the Si wire growth was performed by plasma-enhanced chemical vapor deposition (PECVD), so we benefited from the generation of atomic hydrogen to remove the native aluminium oxide that would prevent any chemical interaction.

---

Fig. 1 The interdigitated solar cell structure. (a) Schematics showing a perspective view of two Al fingers (base contacts) supporting Si p-i-n wires and one Ni finger (emitter contact) supporting NiSi, nanowires (NWs). The p-i-n Si wires are grown first by plasma-enhanced chemical vapor deposition (PECVD). The electrical connection between the n⁺ layer of these Si wires and the emitter bus is made by the NiSi, nanowires that are randomly in contact with the Si wires during the course of their growth, in a second CVD step. (b) A scanning electron microscope (SEM) view of a completed device with interdigitated fingers supporting p-i-n Si wires (top) and NiSi, NWs (bottom). (c) An enlarged SEM view showing the high density of both Si wires and NiSi, NWs on their respective fingers. (d) Another enlarged SEM view showing the high density of contacts between the Si wires and the NiSi, NWs.
between Si and Al.\textsuperscript{16} Since we grow our wires at \(~550\) °C (\textit{i.e.}, below 577 °C which is the Al–Si eutectic temperature) and without any pre-annealing treatment at a higher temperature,\textsuperscript{17} the growth should proceed \textit{via} a vapor–solid–solid (VSS) mechanism.\textsuperscript{18} However, it has been shown recently that phase diagrams on the nanoscale could be different from those corresponding to bulk materials,\textsuperscript{19} thus VLS growth cannot be completely ruled out.\textsuperscript{20} The Al film does not need to be broken into clusters before VLS growth (which would be difficult given its thickness), and wire nucleation is probably initiated on small surface protrusions and hillocks. After growth, we obtain highly tapered Si wires, with the diameters of their top part comparable to the wavelengths of visible light (Fig. S1 & S2, ESI\textsuperscript{†}). This is an ideal situation for minimizing light reflection (see \textit{e.g.}, ref. 1), since due to the tapering of the wires, there is a gradual change of refractive index going from the air down to the roots of the Si wires. During growth, Al is incorporated on substitutional sites into the Si wires\textsuperscript{21} and because it is a group 13 element, p-type doped core Si wires are obtained,\textsuperscript{17,18,22,23} with a doping level that depends on the wire diameter.\textsuperscript{24} The typical carrier concentration in our PECVD-grown Si wires is \(~6 \times 10^{19}\) cm\textsuperscript{−3} (Fig. S3 and S4, ESI\textsuperscript{†}), which is comparable to the values obtained for Al-grown Si wires with large diameters (>70 nm) by Choi and coworkers.\textsuperscript{24} After the conformal deposition of non-intentionally doped a-Si:H (~150 nm thick, \textit{i.e.}, within the range of ambipolar carrier diffusion lengths inside this material, see ref. 25) and n\textsuperscript{+} a-Si:H (see the ESI\textsuperscript{†}, Fig. S2), the unwanted Si between the Al stripes was removed by photolithography and the Ni fingers (250 nm thick) were deposited by lift-off. The samples were reloaded into the PECVD reactor and the growth of the NiSi\textsubscript{x} NWs was performed at \(380\) °C under a flowing mixture of H\textsubscript{2} + SiH\textsubscript{4} without igniting the plasma (see the ESI\textsuperscript{†}). Although many different silicide NWs have been grown in the past,\textsuperscript{26} the synthesis strategy of delivering Si atoms by decomposition of a Si-bearing gas or Si-bearing vapor phase has only been reported for NiSi\textsubscript{x} NWs and more recently for NiGe\textsubscript{x} NWs (with a Ge-bearing gas, see ref. 27).
This synthesis strategy is particularly well adapted to the connection process we describe here. Moreover, NiSi\textsubscript{x} NWs can be grown at a relatively low temperature (380–400 °C or even below, see ref. 28), which is compatible with the stability of the a-Si:H material. Although there are several stable nickel silicide compositions\textsuperscript{26} under our growth conditions, we obtain essentially Ni\textsubscript{3}Si\textsubscript{2} NWs (Fig. S5, ESI\textsuperscript{†}) as formerly assessed.\textsuperscript{29} The resistivity of these NWs is around 80 Ω cm (Fig. S6, ESI\textsuperscript{†}), which corresponds to the value found in thin films of the Ni\textsubscript{3}Si\textsubscript{2} material.\textsuperscript{30} Since the density of NiSi\textsubscript{x} NWs is large, most – if not all – p-i-n Si wires are brought into contact with one or several of such NWs (see Fig. 1c and d); similar pictures taken in other parts of similar devices indicate the same tendency (Fig. S7, ESI\textsuperscript{†}). Note that the unreacted Ni underneath the NiSi\textsubscript{x} layer from which the NWs nucleate and grow.

We point out that for future developments, a metal electrode (e.g., Mo) can be inserted underneath the Ni film to improve conduction.

Fig. 3 presents the electrical characteristics of one of our best p-i-n diode arrays, both in the dark and under 1 sun illumination (1000 W m\textsuperscript{-2}). Most of the light is absorbed in the intrinsic a-Si:H region of the p-i-n wires. Fig. 3b shows the band diagram of the device (see details in Table S1, ESI\textsuperscript{†}). The J–V characteristics in the dark are steeper after the first measurement, indicating contact/resistance improvement due to the annealing effect induced by the current passing through the diode; no more modifications in the J–V characteristics are observed after this first measurement (Fig. 3c). The open circuit voltage (V\textsub{OC}) is 0.67 V and from the dimensions of the active area of the device (144 × 117 μm\textsuperscript{2}, Fig. S8,
ESI†), we extract a photocurrent density $J_{SC} = 8.9$ mA cm$^{-2}$. The fill factor (FF) is 73.8% and the conversion efficiency ($\eta$) is 4.4%. Compared with other solar cells based on Si wires, our efficiency is lower$^{3,7,8}$ but due to our “conservative” photolithography conditions, Si wires represent approximately 33% only of the footprint of the device (see Fig. S2 and S8, ESI†). However, our fill factor value is the highest reported so far for a solar cell based on arrays of CVD-grown Si wires, exceeding the best value obtained in ref. 3 by 6% and the best value obtained in ref. 7 by 16%.

Next, we have evaluated the lateral extension of the NiSi$_x$ NWs by changing the width of the gap between the Al and Ni fingers. Fig. 4 shows that even with a 15 μm-wide gap, we still observe NiSi$_x$ NWs connecting the Si p-i-n wires, although the number of connections is much lower, as evidenced by the ~20 times lower photocurrent value compared with the situation where the gap is 5 μm wide. Hence, under our growth conditions, the maximum lateral extension of the NiSi$_x$ NWs is around 20 μm on each side of a Ni stripe. Having this in mind, it should be possible to design wider Al fingers in the future, thus increasing the percentage of the surface covered with p-i-n Si wires and hence the $J_{SC}$ and the efficiency of the cell.

Since we propose a novel connection principle, we have evaluated the series resistance of one of our best devices, i.e., the one with a 5 μm spacing between the Al and Ni fingers. This has been carried out by plotting $\partial$V/∂I versus I and extracting the slope of the linear part of the curve thus obtained (see the ESI†). As shown in Fig. 5a, we find a series resistance of 0.96 ± 0.03 Ω cm$^{-2}$, which could probably be decreased by decreasing the spacing between the Al and Ni fingers (e.g., down to 2 μm), thus contributing to increasing the fill factor of the cell and its efficiency. This relatively low series resistance value is due to the large number of parallel connections between the base and emitter electrodes; moreover, it is clear from Fig. 1d that each Si wire is brought into contact with several NiSi$_x$ NWs, which tends to reduce the contact resistance. From Fig. 5a, we also find $n = 2.303 \pm 0.004$ for the ideality factor of the p-i-n diodes, a value which is close to those found in p-i-n diodes based on monocrystalline Si NWs.$^{31}$ Finally, using this ideality factor, we have been able to fit the $J$–$V$ characteristics (Fig. 5b) and extract the reverse saturation current at $I_0 \sim 1.18 \times 10^{-7}$ ± 7.3 × 10$^{-10}$ A cm$^{-2}$.

In summary, we have demonstrated a novel connection principle for wire-based solar cells which suppresses the need for any transparent coating. Interestingly, this connection principle essentially relies on random processes: random growth of Si p-i-n wires, random growth of NiSi$_x$ nanowires and random connections between the NiSi$_x$ nanowires and the Si p-i-n wires. Our data have been obtained without particular optimization of the device layout. Still, we report the highest fill factor for a solar cell based on Si wire arrays grown by VLS-CVD. This suggests that the connection principle is interesting enough to continue improving it, in order to achieve efficiency values closer to those predicted for solar cells based on Si wire arrays.

References


